

CLAIMS

WHAT IS CLAIMED IS:

5 1. An interface circuit for operating a capacitive load at a mains supply circuit, in particular a phase gating dimmer, wherein the interface circuit has a first switch, which is designed to short-circuit the input of the load if a mains supply to the input of the load is not effected.

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15 2. The interface circuit as claimed in claim 1, wherein a first transistor is provided as a switch for short-circuiting.

3. The interface circuit as claimed in one of the preceding claims, wherein a second switch is furthermore provided, which is designed to cancel the short circuit of the input of the load if a mains supply to the input of the load is effected.

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4. The interface circuit as claimed in claim 3, wherein the second switch is a second transistor.

25 5. The interface circuit as claimed in claim 4, wherein the base of the second transistor is connected to a respective mains-side input of a rectifier via a first and a second resistor.

30 6. The interface circuit as claimed in one of the preceding claims, wherein a control circuit is provided, which is designed to evaluate a signal generated by the mains supply circuit and to generate a signal for controlling the power consumption of the load.

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7. The interface circuit as claimed in claim 6, wherein the signal of the mains supply circuit is the supply voltage.

8. The interface circuit as claimed in either of claims 6 and 7, wherein the control circuit is designed to generate, on the basis of the duty ratio of the switch, a signal proportional thereto for controlling the power consumption of the load.

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9. The interface circuit as claimed in one of claims 6 to 8, wherein the control circuit has a parallel circuit comprising a series circuit comprising a third resistor and a third transistor, the base of which is connected to the base of the first transistor, a smoothing capacitor and a fourth resistor, the parallel circuit being connected in series with a fifth resistor, the tap of the control signal for the control of the power consumption of the load being provided between the fourth resistor and the fifth resistor.

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10. The interface circuit as claimed in one of the preceding claims, which is embodied separately from load and mains supply in a separate construction.

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11. A circuit arrangement for operating capacitive loads, in particular low pressure discharge lamps, at the mains with a phase gating dimmer, which has a power switch and a timing element, and the capacitive load, wherein an interface circuit as claimed in one of claims 1 to 10 is provided between the load and the phase gating dimmer.

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12. An electronic ballast for a lamp with an integrated interface circuit as claimed in one of claims 1 to 9 for operating at a phase gating dimmer.